TECHNICAL NOTE 166

THE UC1524A INTEGRATED PWM CONTROL CIRCUIT PROVIDES NEW PERFORMANCE LEVELS FOR AN OLD STANDARD

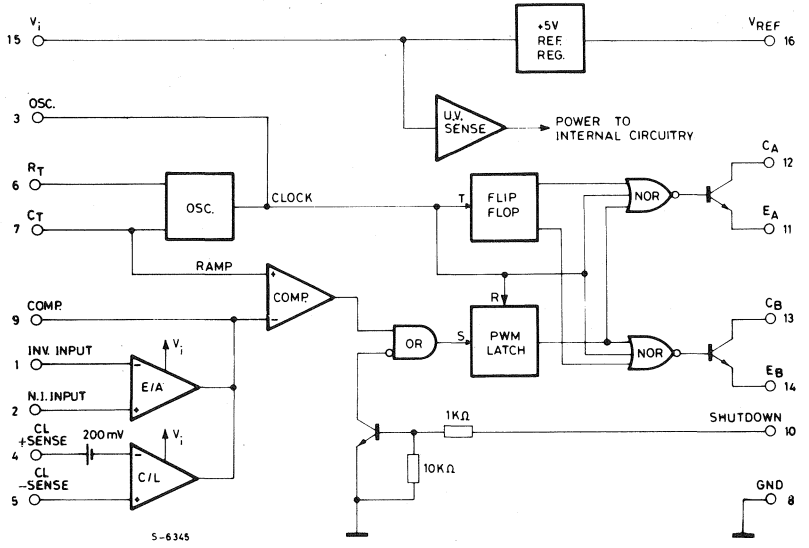
INTRODUCTION

The application of IC technology to the switching power supply really began with the introduction of the SG1524 in 1976. This device was the first IC to implement all the control blocks necessary for a wide range of PWM power systems. Its straight-forward approach to the classic PWM architecture gave it wide acceptance, and it has become the most commonly used IC controller today.

Even though the 1524 has gained great acceptance and engineers have praised its versatile and easy to understand architecture, they have many times cursed the simplistic, or idealistic, ways its individual blocks were implemented. While one would assume, at first glance, that all control functions necessary for most power supply applications are contained within the 1524, in the real word of practical power systems, additional circuitry is required to interface with the rest of the system, to protect against different types of fault conditions, to adjust for inaccuracies, or to improve control during power sequencing.

Although in the intervening years, many new IC control chips have been introduced which offer certain specialized advantages, it was found that

Fig. 1 - The UC1524A block diagram follows the same architecture as the SG1524 but with several significant differences.



design engineers still preferred the 1524 for its wide versatily and generalized architecture. From this understanding, it became apparent that a new design, which would improve many of the 1524's individual functions by making them more predictable and easier to apply, while retaining the same architecture, could be a winner. The result is the UC1524A.

THE UC1524A PWM CONTROLLER

A design goal set for the UC1524A was that it not only retain the same architecture but keep the same pin configuration as the 1524 and function equal to or better than the 1524 in most existing applications. In this way, engineers who were familiar with the 1524 could easily understand and evaluate the UC1524A. Performance improvements had to be significant, particularly in reducing the need for discrete support circuitry, so there would be cost advantage in using the UC1524A in new design. The block diagram of the UC1524A is shown in Figure 1 which, by intent, appears very similar to that of the older 1524.

The list of the improvements, however, is considerable and includes the following:

1. The 5V reference is now internally trimmed to ± 1% accuracy, eliminating the need for potentiometer adjustments.
2. The error amplifier's input range now extends beyond 5V, eliminating the need for a pair of dividers and their attendant tolerances.
3. A high-gain, wide-band, current sense amplifier has been included which is useful for either linear or pulse-by-pulse current limiting in the ground or power supply output lines.
4. An under-voltage lockout circuit has been added which disables all the internal circuitry except the reference until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifyng the design of low-power, off-line converters. There is approximately 600mV of hysteresis included for jitter-free activation.
5. A PWM latch has been added insuring freedom from multiple pulsing within a period, even in noisy environments. In addition, the shutdown circuit feeds direclty to this latch which will disable the outputs within 200ns of activation.
6. The oscillator circuit is usable to frequencies beyond 500KHz and is easier to synchronize with an externa! clock pulse.
7. The power capability of the output switches has been boosted by doubling the current capability to 200mA and increasing the voltage rating to 60V.

An understanding of some of these improvements is necessary for ease in application and will now be discussed in greater detail.

INTERNAL POWER TURN-ON CIRCUIT

The under-voltage lockout and turn-on hysteresis circuit is shown in Figure 2. This circuit requires approximately 2V for activation; but, since nothing else will turn on without at least 3V of supply voltage, lockout is assured. When V_i rises above 2V, R_2 begins to conduct saturating Q_3 and holding the base of Q_5 too low to allow any of the current sources to conduct. The current through R_4 flows through Q_3 and R_3, developing a 600mV drop across R_3 when V_{REF} reaches 5V. At this level, the only current flowing is that used by the reference regulator and R_2 and R_4, a total of approximately 2.5mA at turn-on threshold.

When the input voltage reaches approximately 8V, diode Z begins to conduct turning on Q_2 which turns off Q_3 and allows the current sources to activate. Since the current through Q_2 is much less than through Q_3, the voltage across R_3 drops, providing positive feedback. This gives about 600mV of hysteresis. This circuit, of course, works in reverse at turn off, insuring that the outputs can only operate when the supply is adequate for fully predictable operation. Figure 3 shows the relationship between quiescent current and input voltage. Designers should find this low current start-up characteristic quite advantageous for off-line, primary-side control with boot-strapped operation after turn on.

Fig. 2 — The under-voltage lockout and power turn-on circuitry within the UC1524A

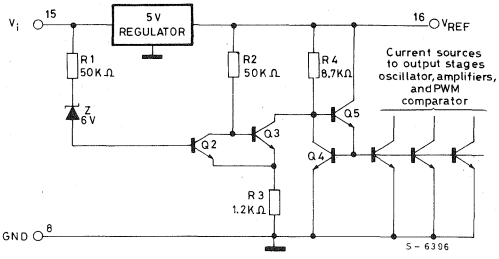


Fig. 3 - Supply current for the UC1524A vs. input voltage

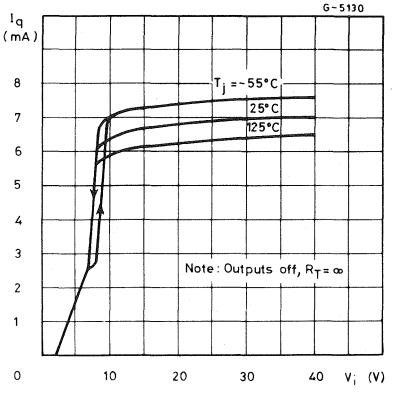
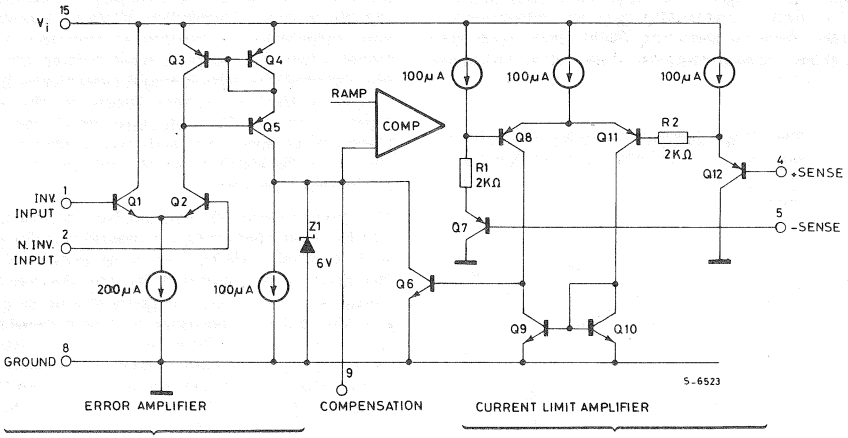


Fig. 4 - Voltage and current sensing amplifiers have a common output at the input to the PWM comparator.



A NEW CURRENT LIMIT AMPLIFIER

Since the outputs of the current limit amplifier and the voltage-sensing error amplifier are summed at the PWM comparator input, they should be examined together as shown in Figure 4.

Since the error amplifier, consisting of transistors Q_1 through Q_5 must have the lowest priority in controlling the PWM, its output must be easily overruled by current faults or other programming functions, such as soft-start, which would hold pin 9 low. Therefore, a transconductance amplifier similar to that used in the earlier 1524 was again applied to the 1524 with one exception: it is now powered by V_i instead of V_{REF}, so that the input common-mode range extends to within 2V of either rail. Zener diode, Z_1, is used on the output to keep the input level to the PWM comparator below 6 volts.

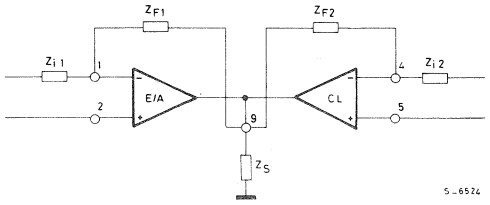
The error amplifier's output can be considered a 100μA current source or sink (0 - 200μA source with 100μA constant sink). When the current limit circuit activates, Q_6 turns on and can easily pull down pin 9 even though the error amplifier would nominally be calling for a high output at this point.

The current limit circuit consists of Q_6 through Q_{12}. Its differential PNP input stage gives it a common mode range extending from 300mV below ground to within -2V of V_i. Its threshold or offset, of 200mV is established by the 100μA current source through R_1, with R_2 added to null out the effect of any base current from Q_8.

This current sensing block within the UC1524A can actually be used either as a linear amplifier or as a comparator. The open loop small-signal gain is approximately 80dB while its transition delay with 10% overdrive is 600ns. This can be decreased substantially with additional overdrive. Use of the current sensing block as a comparator is usually preferred from a systems standpoint, since it does not have to be compensated and pin 9 can be dedicated solely to error amplifier compensation. Under this condition, a current signal over the threshold level will pull pin 9 low, terminating the output signal. Recovery is determined by the 100μA pull-up current from the error amplifier in conjunction with any capacitance which may be present on pin 9.

When the current limit circuit is used as a linear amplifier, stabilization is performed by feedback to the inverting input (pin 4) or by capacitance from pin 9 to ground as shown in Figure 5.

Fig. 5 - Various compensation options which are possible when both amplifiers are operated in the linear mode.

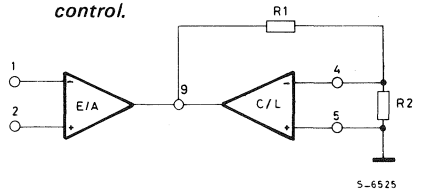


An additional feature of this circuit is its capability to perform as a duty-cycle limiting circuit in the configuration shown in Figure 6. If R_1 is made 100KΩ, there will be minimal effect upon the error amplifier gain.

In current limiting, to achieve the fastest responding pulse-by-pulse control, consideration should be given to the use of the shutdown terminal on pin

10. While the input threshold of this circuit is not as accurately controlled as the current limit amplifier and has a negative temperature coefficient of -2mV/°C and is internally ground referenced; it does feed directly into the PWM latch with only 200ns delay from activation of pin 10 to shutdown of the outputs.

Fig. 6 - The fixed 200mV threshold of the current limit amplifier can be multiplied to form a duty-cycle clamp or dead-band control.



Maximum duty cycle (%) $40\left[0.2\left(\frac{R1}{R2}+1\right)-1\right]$

PWM COMPARATOR AND LATCH

The PWM latch insures only a single pulse is allowed to reach the appropriate output stage within each period. The latch is reset with the oscillator clock pulse which also serves to black the outputs. Thus, although the latch is reset at the start of the oscillator clock pulse, it is the termination of the clock pulse which initiates output conduction. The output then stays on until the latch is set, either by a signal from the PWM comparator or from a shutdown command from pin 10. Once the latch is set, it will hold the output off for the duration of the period.

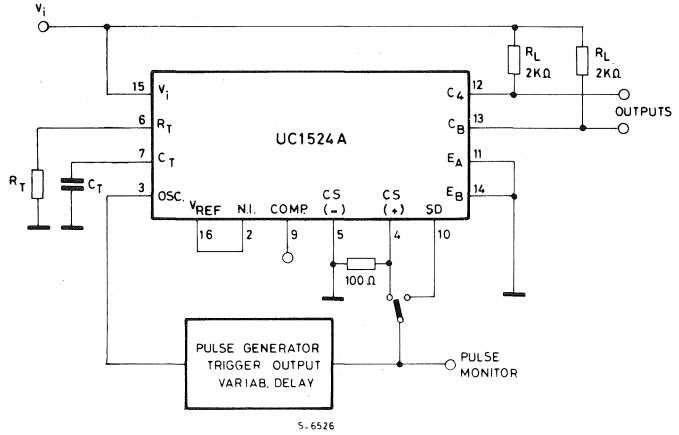
These are several significant advantages to this circuit. First, the latch completely elimitates multiple outputs of the PWM comparator because of noise or ringing on the output of the error amplifier causing multiple crossing of the ramp signal. Second, current limiting can now be performed much more rapidly without instability. Without a latch, significant integration is needed to maintain a turn-off signal after the outputs have turned off. Finally, any instabilities which might potentially be present in the voltage or current loops, or the shutdown signal from pin 10, will cause much less stress on the output stages, since only two transitions through the high-dissipation active region can be made during each period.

The performance or this portion of the UC1524A can be evaluated using a triggerable pulse generator with a variable delay, set up as shown in Figure 7. R_T and C_T are selected for the desired operating frequency. The clock triggers the pulse generator, and the delay is adjusted so the generator output occurs during the PWM period. The output pulse width must be at least 200ns and the amplitude higher than the threshold of the UC1524A input being evaluated. Typical waveform photographs are shown in Figure 8.

HIGHER POWER OUTPUT SWITCHES

With the higher current and voltage rating of the UC1524A's output switches, significant economies can now be achieved in interfacing with higher power devices. For low power requirements, a broader range of applications may now be served by the 1524A itself without additional discrete output devices. Regardless of the power supply requirement, more current and voltage from the UC1524A will ease the design tradeoffs. Even with higher current and voltage, the UC1524A offers fast response time. Each output stage contains an anti-saturation network to keep the output transistors out of hard saturation. Although this adds somewhat to the saturation voltage, it is more than offset by the benefits in reducing turn-off delay.

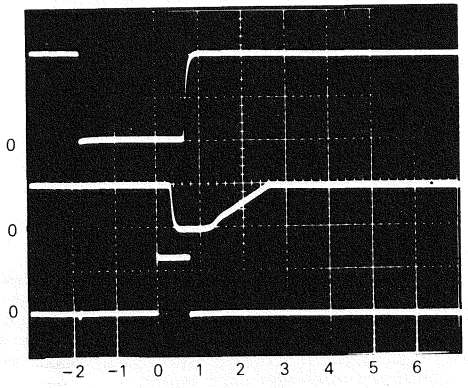
Fig. 7 - Evaluating the turn-off delays of the UC1524A with the aid of a triggerable pulse generator with variable delay.



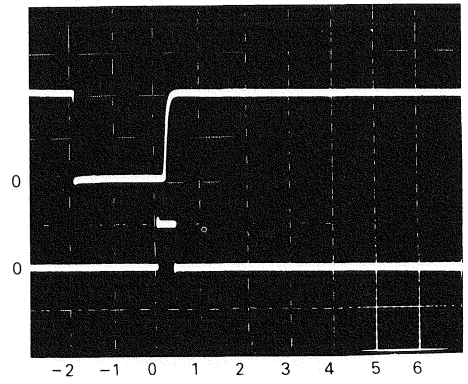
Saturation voltage as a function of current is shown in Figure 9.

Since both collectors and emitters are available on the UC1524A's output transistors, many different coupling possibilities are offered. One useful configuration for enhanced turn-off is shown in Figure 10. The fast-rising signal appearing at the collector of the output transistor, Q_1, is capacitively coupled to saturate an external transistor, Q_2, greatly reducing the turn-off delay of Q_3 and allowing a much larger value to be selected for R_3. Many variations of this circuit are possible depending upon the power devices to be driven and the voltage levels required.

Fig. 8 - Typical turn-off response from both the current sense and shutdown inputs.



Top — Output, 10V/div
Middle — Comp output, 5V/div
Lower — Current sense input, 200mV/div
Time — 1μs/div



Upper — Output, 10V/div
Lower — Shutdown input, 1V/div
Time — 1μs/div

Fig. 9 - Output saturation characteristics for each of the UC1524A's outputs.

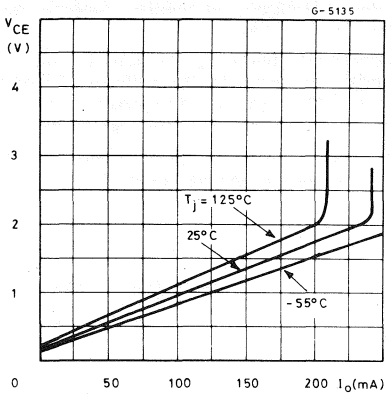
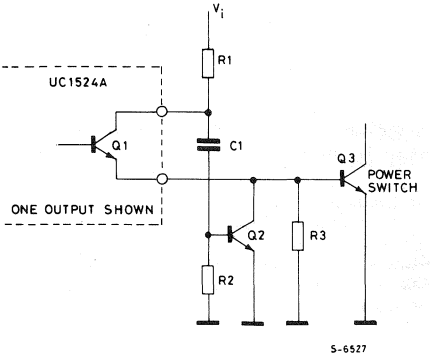


Fig. 10 - The addition of C_1 and Q_2 uses the collector signal of the UC1524A to generate an enhanced turn-off command for Q_3



FREQUENCY SYNCHRONIZATION

The oscillator circuit within the UC1524A, shown in Figure 11, has been improved over that of the 1524 with the addition of C_2. Without this component a synchronizing pulse externally applied to pin 3 had to do all the work of discharging the timing capacitor through Q_4 and Q_5. The simple addition of C_2 couples a positive pulse from pin 3 to the base of Q_{10}, momentarily reducing the threshold of comparator Q_8-Q_9 and regeneratively triggering the oscillator into its discharge state. The circuit is now leading-edge triggered and narrow pulses can be used. This is a consideration when minimum dead time is required, since the outputs are blanked off as long as pin 3 is held high.

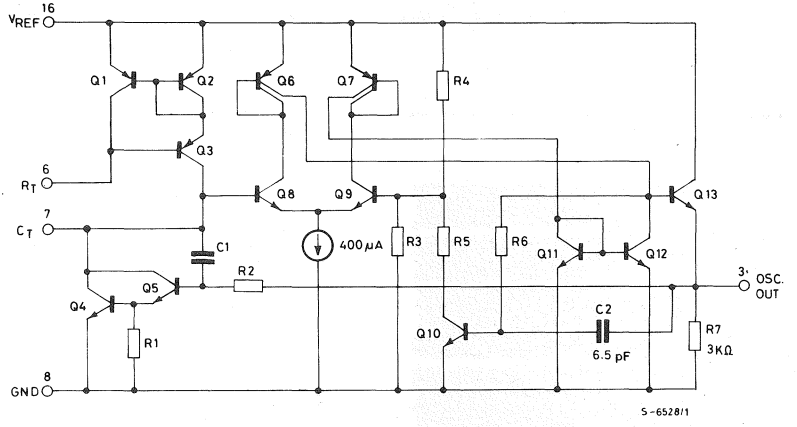
As with the 1524, synchronization to an external clock should be done with the R_T C_T time constant set approximately 10 to 20% greater than that determined for the required clock frequency, taking into consideration the expected tolerances of the

components. For synchronizing multiple UC1524A devices, all R_T, C_T, and OSC output terminals should be individually connected together and a single R_T and C_T used.

When considering blanking, the pulse on pin 3 may be extended somewhat by the addition of a capacitor of up to 100pF from pin 3 to ground. If narrower blanking pulses are required, adding a resistive load from pin 3 to ground of 1KΩ minimum will reduce the pulse width.

The best way to guarantee a large dead time is still to use a diode to clamp the peak output from the error amplifier to a divider from V_{REF}. This technique is quite accurate due to the accuracy of V_{REF} and the 100μA fixed current available from the amplifier.

Fig. 11 - The oscillator circuit of the UC1524A allows both high frequency operation and ease of external synchronization.



A COMPLETE DC-DC CONVERTER WITH THE UC1524A

An important attribute of the new UC1524A family is the higher voltage rating on the output transistors. This now makes it possible to implement a practical 4W DC-DC converter operating from a common 28V bus with no additional output transistors. The schematic of Figure 12 uses a push-pull configuration which imposes a voltage of twice the supply across the "OFF" transistor. This is now within the rating of the UC1524A and, thus, with a 28 : 7 turns ratio in the transformer, a 5V, ¾A output is achieved with 78% efficiency at a significant minimum parts count.

The fast response of the current limit amplifier within the UC1524A again keeps the device well protected as shown in the waveforms of Figure 13.

Fig. 12 - With higher output voltage capability, the UC1524A can implement a complete 4W DC to DC converter with no additional switching transistors.

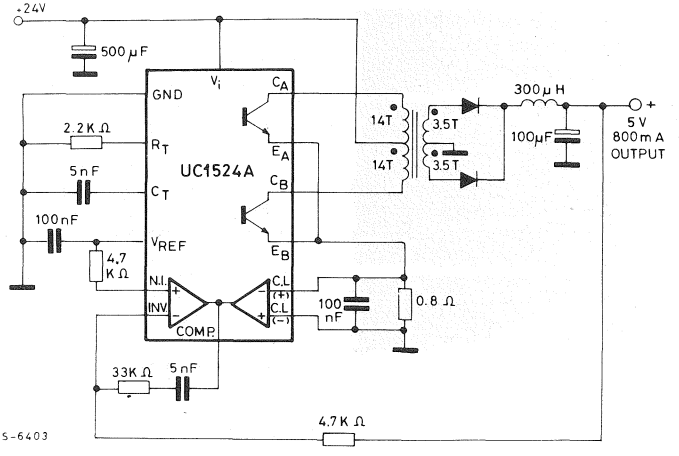
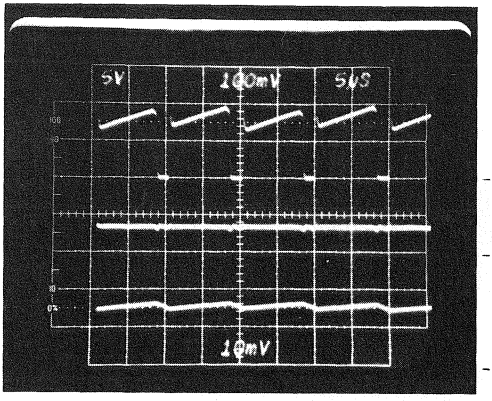
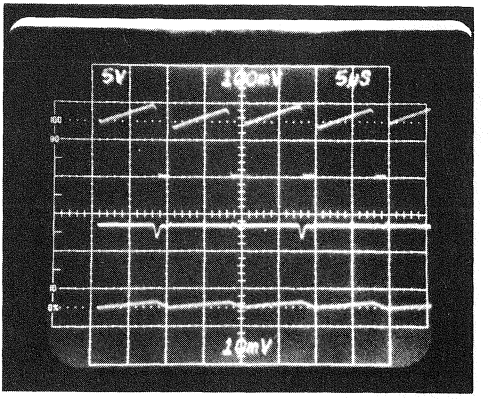


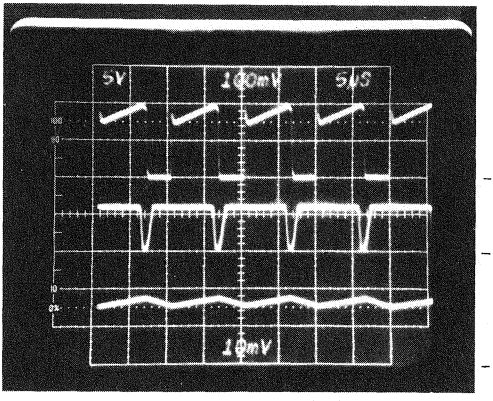
Fig. 13 - Operating waveforms for the PWM DC-DC converter (Fig. 12)
Upper trace = Primary current at 0.1A/division
Middle trace = Pin 9 voltage at 5V/division
Lower trace = Load current at 0.5A/division
Time base = 5µs/division



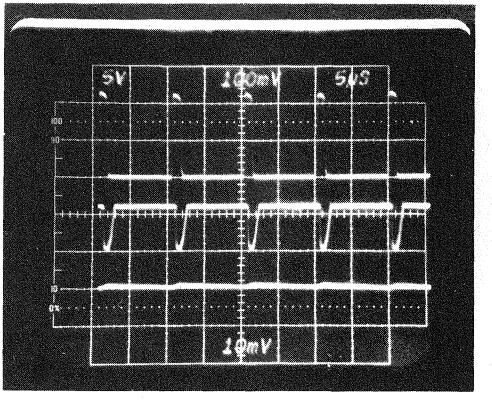
Circuit under normal load



Circuit at threshold of current limiting



Circuit under full current limit



Circuit under short circuit conditions

AN OFF-LINE FORWARD CONVERTER

For low to medium power application single-ended flyback or forward converter with all the control on the primary side of the isolation step-down transformer is usually the most economical solution. However there are two complications with this approach. The first is that although the control circuitry can easily be driven from a low-voltage winding on the power transformer, starting energy must be taken from the high-voltage rectified line where, at 170VDC, every 10mA represents a 1.7W loss. The second complication is in obtaining adequate regulation of the output while still meeting isolation requirements from output back to the line.

The 50W forward converter of Figure 14 offers innovative solutions to both these problems. In this circuit, the UC1524A provides all the control with its operating drive power coming from winding N_2. The low-current start-up characteristics of the UC1524A allow starting energy to be developed in C_2 with only approximately 8mA required through R_1.

The problem of isolated feedback control is solved in this application by sampling the 5V output level at the switching frequency be means of the 2N2222 transistors and transformer T_2. With every switching cycle, the output voltage is transferred from N_1 to N_2 where it is peak detected to generate a primary-referenced signal to drive the PWM

Fig. 14 - This 50W off-line forward converter features both high efficiency and good regulation while maintaining input-output isolation.

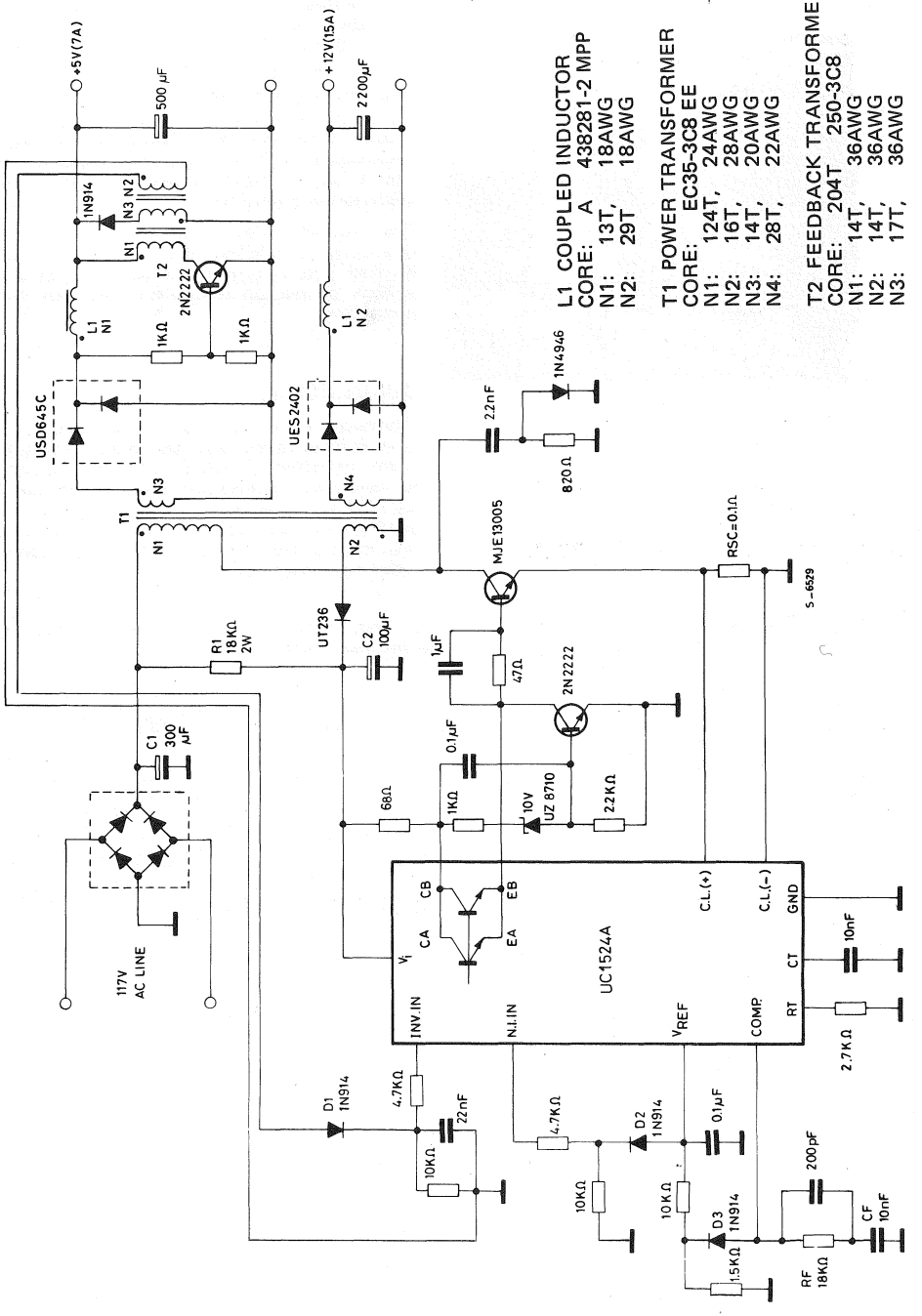
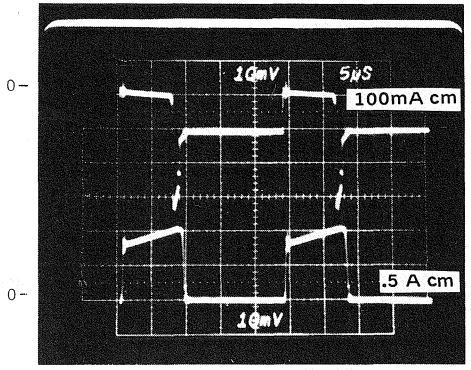


Fig. 15 - Base current (upper trace) and collector current for the MJE13005 of fig. 14. The time base is 5μs per division



at Full Load (50W)

error amplifier. Diode D_2 is used to temperature compensate for the loss in the rectifier, D_1 and the net result is better than 1% regulation with the main added cost that of a very inexpensive signal transformer.

Some of the other features of this application include a duty-cycle clamp on the PWM formed by diode D_3 and the 10K - 1.5K divider from V_{REF}. This method of clamping is more effective with the UC1524A since the UV lockout keeps the outputs off until the reference, error amplifier, and oscillator are all operating within specification.

Drive for the MJE13005 high-voltage switch is accomplished by using the emitters of the UC1524A's output transistors for turn-on and the 2N2222 in conjunction with the 1μfd base capacitor to provide a negative base voltage for rapid turn-off as described in Figure 10.

The resultant drive signal is shown in Figure 15. Operating at 40KHz, this regulator provides an isolated 50W of power with an efficiency of 83% , a high degree of regulation, and fast overload protection.

CONCLUSION

Although there are now many new integrated circuits from which to choose in attempting to build more cost-effective power supplies, it always helps to review well established ideas. In the case of the UC1524A, updating and improving an earlier product has resulted in a significant advancement providing greater performance and versatility while reducing system costs.

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